Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A**
2. **B**
3. **J**
4. **K**
5. **C**
6. **D**
7. **VSS**
8. **E**
9. **F**
10. **L**
11. **M**
12. **G**
13. **H**
14. **VDD**

**.058”**

**13**

**14**

**1**

**12 11 10 9**

**8**

**7**

**2 3 4 5 6**

**CD4001UB**

**MASK**

**REF**

**.053”**

**Top Material: Al**

**Backside Material: SiN4**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: CD4001UB**

**APPROVED BY: DK DIE SIZE .053” X .058” DATE: 9/6/18**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD4001UB**

**DG 10.1.2**

#### Rev B, 7/1